The following is a complete listing of all claims in the application, with an indication of the status of each:

Listing of claims:

1. (currently amended) A method of forming a field effect transistor (FET), comprising:

providing a substrate;

forming a layer on the substrate, the layer having exposed vertical side surfaces on opposite sides of the layer;

forming an epitaxial channel on ~~the~~ each of the exposed vertical side surfaces of the layer, the channel having an exposed first vertical sidewall opposite the vertical side surface of the layer;

removing a channel on a first vertical side surface of the layer and then removing the layer, thereby exposing a second vertical sidewall of the channel formed on the second vertical side of the layer;

forming a second channel in place of said removed channel; and

forming a gate adjacent to at least one of the sidewalls of the channel and the second channel, there being a gate dielectric between each channel and the gate.

2. (withdrawn) A field effect transistor (FET) comprising:

a substrate;

a source region and a drain region in the substrate, each of said source region and said drain region having a top, bottom and at least two side diffusion surfaces, the source and drain regions separated by an epitaxially

grown channel region having a top, bottom and side channel surfaces substantially coplanar with corresponding ones of the diffusion surfaces;

a gate adjacent the top and the side channel surfaces and electrically insulated from the top and side channel surfaces; and

the gate comprising a planar top surface, the planar top surface having a contact for receiving a gate control voltage for controlling the FET.

3. (withdrawn) The FET as recited in claim 2, wherein the source and drain have a contact for receiving a control voltage for controlling the FET.

4. (withdrawn) The FET as recited in claim 2, wherein the gate is substantially centered between and substantially parallel to said source region and said drain region.

5. (withdrawn) The FET as recited in claim 2, further comprising a silicide layer that contacts a top surface of said gate.

6. (withdrawn) The FET as recited in claim 2, further comprising a dielectric layer that contacts a first side end and a second side end of said gate.

7. (withdrawn) The FET as recited in claim 2, further comprising a dielectric that contacts side surfaces of the channels.

8. (withdrawn) The FET as recited in claims 2, where the gate is comprised of polysilicon.

9. (withdrawn) The FET as recited in claim 2, wherein the channel is approximately one fourth of a length of the FET.

10. (withdrawn) The FET as recited in claim 2, further comprising a dielectric material in the gate for electrically separating the gate into two electrically isolated portions, each having a substantially coplanar top surface and a contact pad on each respective substantially coplanar top surface.

11. (withdrawn) The FET as recited in claim 2, wherein said epitaxial channel is formed of a combination of Group IV elements.

12. (withdrawn) The FET as recited in claim 2, wherein said epitaxial channel is formed of an alloy of silicon and a Group IV element.

13. (withdrawn) The FET as recited in claim 2, wherein said epitaxial channel is formed of an alloy of silicon and at least one of germanium and carbon.

14. (currently amended) A method for forming a double gated field effect transistor (FET), comprising the steps of:

forming on a substrate a first and a second epitaxially grown channels, said channels having vertical side surfaces extending up from the substrate, wherein said second channel is grown following removal of a ~~central~~ semiconductor region centered between said channels upon ~~which one of~~ whose opposite vertical sides said first channel was grown;

etching areas within a silicon layer to form a source and a drain, wherein a side surface of the source and the drain contact opposing end surfaces of the first and second epitaxially grown channels; and

forming a gate that contacts a top surface and two side surfaces of the first and second epitaxially grown channels and a top surface of the substrate.

15. (previously presented) The method as recited in claim 14, wherein the forming step comprises the steps of:

forming first and second semiconductor lines, each end of the silicon lines contacting an end of the source and the drain;

forming an etch stop layer on an exposed side surface of each of the first and second semiconductor lines;

epitaxially growing first and second semiconductor layers on each etch stop layer;

etching away the first and second semiconductor lines and the etch stop layers;

filling areas surrounding the first and second epitaxially grown semiconductor layers and between the source and the drain with an oxide fill; and

etching a portion of the oxide fill to form an area that defines a gate, wherein the area that defines the gate is substantially centered between and substantially parallel to the source and the drain.

16. (original) The method as recited in claim 15, further comprising the steps of:

etching the oxide fill between the gate the source to expose the first and second epitaxially grown silicon layers; and

etching the oxide fill between the gate and the drain to expose the first and second epitaxially grown silicon layers.

17. (original) The method as recited in claim 16, further comprising the step of forming an oxide on the first and second epitaxially grown silicon layers.

18. (original) The method as recited in claim 17, wherein the oxide is silicon dioxide.

19. (previously presented) The method as recited in claim 14, further comprising the steps of:

implanting a portion of the epitaxially grown silicon layers between the gate and the source; and

implanting a portion of the epitaxially grown silicon layers between the gate and the drain.

20. (previously presented) The method as recited in claim 19, wherein the implanting step is in the range of 10 to 45 degrees relative to a vector perpendicular to a top surface of the epitaxially grown silicon layers.

21. (previously presented) The method as recited in claim 20, wherein the implants are done in a series at approximately 90 degrees relative to each other.

22. (original) The method as recited in claim 14, further comprising the step of forming a contact on each of the gate, the source and the drain.

23. (original) The method as recited in claim 14, wherein the gate material is polysilicon.

24. (previously presented) A method of forming an FET, comprising:

forming on a substrate a first semiconductor layer having first and second ends and a central region that is thinner than said first and second ends,

said central region having first and second side surfaces extending upward from said substrate;

epitaxially growing a semiconductor channel region on at least one of said first and second side surfaces of said central region of said first semiconductor layer, a first side of said channel being exposed;

removing said central region of said first semiconductor layer, thereby exposing a second side of said channel;

forming a dielectric layer on exposed surfaces of said semiconductor channel region; and

forming a gate electrode on said dielectric layer.

25. (previously presented) The method of claim 24, wherein said semiconductor channel region is formed of a combination of Group IV elements.

26. (previously presented) The method of claim 24, wherein said semiconductor channel region is formed of an alloy of silicon and a Group IV element.

27. (previously presented) The method of claim 24, wherein said semiconductor channel region is formed of a material selected from the group consisting of silicon, silicon-germanium, and silicon-germanium-carbon.

28. (previously presented) The method of claim 27, wherein said step of removing said first semiconductor layer does not appreciably remove said semiconductor channel region.

29. (previously presented) The method of claim 28, wherein an etch stop is epitaxially grown between said first semiconductor layer and said semiconductor channel region.

30 (previously presented) The method of claim 24, wherein said gate electrode is formed of a material selected from the group consisting of polysilicon, silicon-germanium, refractory metals, Ir, Al, Ru, Pt, and titanium nitride.